

**Complete if Known**

(use as many sheets as necessary)

Sheet 1 of 3

<b>Application Number</b>	Not yet assigned
<b>Filing Date</b>	June 20, 2001
<b>First Named Inventor</b>	Keeth et al.
<b>Group Art Unit</b>	Not yet assigned
<b>Examiner Name</b>	Not yet assigned
<b>Attorney Docket Number</b>	DB000575-012

100-474118-PTO

06/20/01  


Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
EW		6,043,118		Suwanai et al.	03/28/2000	
		5,960,455		Bauman	09/28/1999	
		5,838,627		Tomishima et al.	11/17/1998	
		5,677,645		Merritt	10/14/1997	
		5,651,011		Keeth	07/22/1997	
		5,614,859		Ong	03/25/1997	
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		5,557,579		Raad et al.	09/17/1996	
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		5,379,263		Ogawa et al.	01/03/1995	
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		5,231,605		Lee	07/27/1993	
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[illegible]

5/2/02

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PTO/SB/08B (08-00)

App. for use through 10/31/2002. OMB 0651-0031

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Substitute for form 1449B/PTO			<b>Complete if Known</b>		
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			Application Number	Not yet assigned	
			Filing Date	June 20, 2001	
			First Named Inventor	Keeth et al.	
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			Examiner Name	Not yet assigned	
			Attorney Docket Number	DB000575-012	
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
GT		SUGIBAYASHI ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
GT		TAGUCHI ET AL., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26 (No. 11), (November 1991)	
GT		KITSUKAWA ET AL., "256-Mb DRAM Circuit Technologies for File Applications", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
GT		JEDEC SOLID STATE PRODUCTS ENGINEERING COUNCIL, "Committee Letter Ballot", JC-42.3-95-73, Item #633.13, Arlington, VA (April 1995)	
GT		YOO ET AL., "SP 23.6: A 32-Bank 1Gb DRAM with 1 GB/s Bandwidth", ISSCC96/Session 23/DRAM/PAPER SP 23.6	
GT		NITTA ET AL., "SP 23.5: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", ISSCC96/Session 23/DRAM PAPER SP 23.5	
GT		U.S. Patent Application S.N. 08/521,563, entitled IMPROVED VOLTAGE REGULATOR CIRCUIT, filed 8/30/95	
GT		U.S. Patent Application S.N. 08/668,347, entitled DIFFERENTIAL VOLTAGE REGULATOR, filed 6/26/96	
GT		U.S. Patent Application S.N. 08/460,234, entitled SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY, filed 8/17/95	
GT		U.S. Patent Application S.N. 08/420,943, entitled DYNAMIC RANDOM-ACCESS MEMORY, filed 6/4/95	
GT		U.S. Patent Application S.N. 08/194,184, entitled INTEGRATED CIRCUIT POWER SUPPLY HAVING PIECEWISE LINEARITY, filed 2/8/94	

Examiner Signature		Date Considered	5/21/02
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<sup>1</sup> Unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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